What is claimed is:

1. A circuit for selecting one of a second set of binary inputs according to the number of high input signals applied to a first set of one or more binary inputs, the circuit comprising:

a first subcircuit having said first set of binary inputs, and logic for generating a set of control output signals, wherein each control output signal represents whether or not the first set of binary inputs has exactly a predetermined number of high input signals, and wherein each control output signal corresponds to a different said predetermined number of high input signals; and

a second subcircuit having said second set of binary inputs, a set of control inputs for receiving control output signals from the first subcircuit, and logic comprising a plurality of switching components including one or more pass gates, each said switching component being switchable to connect or isolate one of the second set of inputs to a common output, wherein the control inputs are connected to control the switching of the switching components to connect only one of said second set of binary inputs to said common output at any one time.

2. A circuit as claimed in claim 1, wherein said switching components include one or more transistors, each said transistor being connected to receive an input from a constant high or low voltage source.

3. A circuit as claimed in claim 1, wherein the number of control output signals of the first subcircuit is one greater than the number of binary inputs in the first set of binary inputs.

4. A circuit as claimed in claim 1, wherein the set of control inputs of the second subcircuit are connected to control the switching elements, in a one-to-one correspondence between control inputs and switching elements.

5. A circuit as claimed in claim 1, wherein the first subcircuit is configured to generate only a single high control output signal at any time.

6. A circuit as claimed in claim 1, wherein the first subcircuit is configured to generate only a single low control output signal at any time.

7. A circuit as claimed in claim 1, wherein said set of control inputs of the second subcircuit consists of a single control input, and the second subcircuit comprises an inverter having an input connected to said single control input, wherein said single control input is connected to control a first switching component, and an output of the inverter is connected to control a second switching component.

8. A circuit as claimed in claim 1, wherein said switching components are connected to said common output via low output impedance buffer means.

9. A circuit as claimed in claim 8, wherein said low output impedance buffer means comprises an inverter.

10. A circuit as claimed in claim 1, further comprising a third subcircuit, the third subcircuit having a third set of binary inputs and logic to generate one or more output signals indicating if the number of highs or lows amongst the third set of binary inputs belongs to a particular subset of the integers $\{0, \ldots, n\}$, each said output signal corresponding to a different particular subset of the integers $\{0,\ldots,n\}$, wherein n is the number of binary inputs in the third set of binary inputs, and wherein one or more of the second set of binary inputs of the second subcircuit is connected to receive an output signal from the third subcircuit.

11. A circuit as claimed in claim 10, wherein said logic of the third subcircuit is adapted such that only one said output signal from the third subcircuit is high at any time.

12. A circuit as claimed in claim 10, wherein said logic of the third subcircuit is adapted such that only one said output signal from the third subcircuit is low at any time.

13. A circuit as claimed in claim 10, wherein said particular subset of the integers {0,...,n} comprises a single integer.

14. A circuit as claimed in claim 13, wherein each of a plurality of said control inputs of the second subcircuit indicate whether a respective number p of highs are present amongst the first set of binary inputs and is connected to control a respective switching element with an input indicating whether a respective number of at least q highs are present amongst the third set of binary inputs, wherein the sum of p and q has the same value for each of said plurality of switching elements.

15. A circuit as claimed in claim 10, wherein said particular subset of the integers {0,...,n} comprises all integers greater than or equal to a predetermined integer and less than or equal to n.

16. A circuit as claimed in claim 15, wherein each of a plurality of said control inputs of the second subcircuit indicate whether a respective number p of highs are present amongst the first set of binary inputs and is connected to control a respective switching element with an input indicating whether a respective number of at least q highs are present amongst the third set of binary inputs, wherein the sum of p and q has the same value for each of said plurality of switching elements.

17. A circuit as claimed in claim 14, wherein a plurality of second subcircuits are provided to generate a plurality of third subcircuit outputs, each second subcircuit corresponding to a different sum of p and q.

18. A circuit as claimed in claim 16, wherein a plurality of second subcircuits are provided to generate a plurality of third subcircuit outputs, each second subcircuit corresponding to a different sum of p and q.

19. A logic circuit including the circuit of claim 14, said logic circuit having inputs arranged in a tree structure, wherein at each level of the tree a plurality of first and third

subcircuits accept level inputs to said level and a plurality of third subcircuits each accept inputs from a first and third subcircuit and generate a signal for input to the next level of the tree.

20. A logic circuit including the circuit of claim 16, said logic circuit having inputs arranged in a tree structure, wherein at each level of the tree a plurality of first and third subcircuits accept level inputs to said level and a plurality of third subcircuits each accept inputs from a first and third subcircuit and generate a signal for input to the next level of the tree.

21. A parallel counter comprising at least one circuit according to claim 1.

22. A parallel counter comprising:

a plurality of lower level logic units each having the circuit of claim 14; and

a plurality of higher level logic units each having a circuit with two sets of binary inputs, an output, and logic connecting the binary inputs to the output, the logic being for generating an output signal indicating if the total number of highs or lows amongst the two set of inputs belongs to a particular subset of the integers {0, ..., n} wherein n is the total number of inputs in the two sets of inputs;

wherein said logic units are arranged hierarchically such that the output of the lower level logic units is passed to higher level logic units.

23. A parallel counter comprising:

a plurality of lower level logic units each having the circuit of claim 16; and

a plurality of higher level logic units each having a circuit with two sets of binary inputs, an output, and logic connecting the binary inputs to the output, the logic being for generating an output signal indicating if the total number of highs or lows amongst the two set of inputs belongs to a particular subset of the integers {0, ..., n} wherein n is the total number of inputs in the two sets of inputs;

wherein said logic units are arranged hierarchically such that the output of the lower level logic units is passed to higher level logic units.

24. A parallel counter comprising a plurality of circuits according to claim 14, wherein said plurality of circuits are arranged hierarchically such that the first and third subcircuit of each higher level circuit comprises a lower level circuit.

25. A parallel counter comprising a plurality of circuits according to claim 16, wherein said plurality of circuits are arranged hierarchically such that the first and third subcircuit of each higher level circuit comprises a lower level circuit.

26. A parallel counter comprising the circuit of claim 14, wherein the binary inputs of said second set of inputs and said first set of inputs are divided according to a binary tree into inputs to a plurality of logic units.

27. A parallel counter comprising the circuit of claim 16, wherein the binary inputs of said second set of inputs and said first set of inputs are divided according to a binary tree into inputs to a plurality of logic units.

28. A logic circuit including the parallel counter of any one of claims 21 to 27.

29. An integrated circuit including the parallel counter of any one of claims 21 to 27.

30. A multiplier circuit comprising a parallel counter according to any one of claims 21 to 27.

31. A memory control circuit comprising a circuit according to claim 1.

32. A circuit board comprising the circuit of claim 1.

33. A digital electronic device including the circuit of claim 1.